IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re application of

THEODORE W. HOUSTON

Serial No. 09/346,436 (TI-21004)

Filed July 1, 1999

For: BONDED SOI WITH BURIED INTERCONNECT TO HANDLE OR DEVICE WAFER

Art Unit 2813

Examiner E. Kielin

Commissioner for Patents
Washington, D. C. 20231

Sir:

SUBSTITUTE SUPPLEMENTAL APPEAL BRIEF

In reply to (1) the Notice of Non-Compliance, (2) the new final rejection which is couched as a Supplemental Examiner's Answer, replacing the Supplemental Appeal Brief, and (3) in accordance with the directive therein at page 2, the appeal is hereby reinstated as set forth in the Reply Brief. In other words, the appealed claims are claims 9 and 22 with claims 25 and 26 having been objected to but stated to contain allowable subject matter. Since all claims have been canceled by not having been appealed with the exception of claims 9 and 22, which remain on appeal and claims 25 and 26 which have been stated to be allowable if independently presented, this appeal only involves claims 9 and 22. Accordingly, the Supplemental Appeal Brief was in compliance with 37 C.F.R. 1.192(c). Claims 9 and 22 are reproduced and attached hereto for the convenience of the

Board. Out of an abundance of caution and to clarify the issues in this application, all claims are herewith cancelled with the exception of claim 9 and 22 which are on appeal and claims 25 and 26 which have been indicated to be allowable.

With reference to claim 9 (and also claim 22), the Examiner states that "[m]erely pointing out differences is not an argument as to why the claims are separately patentable". This argument fails for at least two reasons. First, since the rejection is based upon 35 U.S.C. 102(b), it is incumbent that each and every step claimed and each and every function of the claimed step be found in a single reference. This is not the case as has been demonstrated in the Brief on Appeal and in the Reply Brief. It follows that if the section of 37 C.F.R. quoted by the Examiner is to be interpreted as the Examiner does, that it contradicts 35 U.S.C. 102(b) and is invalid. Therefore, it must be assumed that this section does not apply to 35 U.S.C. 102. Secondly, it should again be noted that the rejection involved in Issue 1 which relates to the rejection of claim 9 is based upon 35 U.S.C. 102(b). This requires that each and every step claimed as well as the function set forth for each step be set forth in the cited reference, namely Hayashi (U.S. 5,087,585). This is not the case for claim 9 which requires that the electrical interconnect structure in the electrically insulating layer contact both the device layer and the substrate and, as stated in claim 9 "form an electrical interconnect structure in said electrically insulating layer, said interconnect structure contacting both said device layer and said substrate". The interconnect structure of Hayashi is the metal pool which is not disposed in the electrically insulating layer and therefore there can be no interconnect in the electrically insulating layer of Hayashi which contacts both the device layer and the substrate. The "interconnect" of Hayashi is disposed in an opening formed in the electrically insulating

layer 17. This contact is, in fact, only later made when the refractory metal bump later contacts the metal pool. Accordingly, not only are the claimed steps not all found in Hayashi, but, in addition, the order of the steps as specifically claimed in the combination of claims 7 and 9 is not met by Hayashi. These facts have nowhere been refuted in the new final rejection.

With reference to the rejection of claims 1, 3, 7 to 9, 18 to 21, 23 and 24, this rejection cannot be understood since all of these claims with the exception of claims 9 and 22 have been canceled. Accordingly, the argument presented above applies to claim 9 and is repeated.

With regard to the rejection of claims 1 to 4, 7 to 9 and 18 to 24 under 35 U.S.C. 103(a) as being unpatentable over Hayashi in view of APA, Issue 2, it is again noted that only claims 9 and 22 remain on appeal. The argument presented above with reference to claim 9 applies as well to this rejection of claim 9. As to claim 22, there is no so-called admission in Appellant's Admitted Prior Art (APA) that it is even known that the oxide will always appear in the process as claimed, let alone that it be known to remove such oxide, especially in the environment as claimed. Accordingly, this rejection is not based upon the record and clearly not upon APA.

In view of the above, the appeal remains as to claims 9 and 22 with claims 25 and 26 having been indicated to be allowable. Reversal of the final rejection of claims 9 and 22 is therefore urged that justice be done in the premises.

Respectfully submitted,

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APPENDIX

The claims on appeal are claim 9 and 22 with claims 7 and 18 being included because claims 9 and 22 depend therefrom, it being noted that claims 7 and 18 are not on appeal per se.

7. A method of forming an SOI structure, comprising the steps of:

providing a device layer having at least one of active or passive elements on a surface thereof;

providing a substrate having at least one of active or passive elements on a surface thereof;

providing an electrically insulating layer having an interconnect structure disposed therein and extending to a surface thereof;

forming a substantially planar region on said surface of said device layer and said surface of said substrate;

forming a substantially planar region on said surface of said electrically insulating layer;

interposing said electrically insulating layer between said device layer and said substrate with said planar region of said electrically insulating layer overlaying said substantially planar region on said at least one of said surface of said device layer and said surface of said substrate to make electrical contact with a device in at least one of the device wafer and the substrate; and

then bonding said planar surface of said electrically insulating layer to said overlying one of said substrate and said device layer.

9. The method of claim 7 further including the step of forming an electrical interconnect structure in said electrically insulating layer, said interconnect structure contacting both said device layer and said substrate.

18. A method of fabricating an integrated circuit which comprises the steps of:

(a) providing a device layer having at least one of active or passive elements on a surface thereof;

(b) providing a substrate having at least one of active or passive elements on a surface thereof;

(c) providing a dielectric bonded to one of said device layer and said substrate having an interconnect disposed therein and extending to at least one surface thereof;

(d) then bonding said dielectric to the other of said device layer and said substrate to form an interface with said one of said device layer and said substrate and forming an electrically conductive path across said interface to said interconnect.

22. The method of claim 18, further including a dielectric disposed over said interconnect at said interface preventing electrical conduction across said interface, wherein said step of forming an electrically conductive path across said interface to said interconnect is formed by breakdown of said dielectric.